## ABSTRACT OF THE DISCLOSURE

Input/output cells are formed so as to be peripherally arranged adjacent to a corner cell on a surface of a semiconductor chip, and electrode pads are formed on the respective input/output cells. The electrode pads are configured in a zigzag pad arrangement so as to form inner and outer pad arrays. However, of the electrode pads forming the inner pad array, those electrode pads in predetermined areas adjacent to the two sides of the corner cell are not disposed, such that an interconnect pattern of a carrier which is bump-bonded to the semiconductor chip and vias are prevented from becoming complex.